

REMARKS

The objections, rejections and comments of the Examiner set forth in the Office Action dated July 21, 2003 have been carefully reviewed by the Applicant.

Claims 6-8 are objected to for lacking a complete description of the act of "distributing." In response, "distributing" has been changed to "distributing events in the primary event stream" per the requirements of the Examiner.

Claims 1 and 10 are currently rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (US 5642478). In response, Claims 1 and 10 have been amended to more clearly distinguish the present claimed invention from Chen. Specifically, Claims 1 and 10 have been amended to include timestamping an event with a resolution of less than one clock cycle.

Paragraph 0005 of the present specification defines a timestamp as a digital representation of the time at which an event occurs. The digital representation of the time at which an event occurs has two components. The first component is the

specific clock cycle of the reference clock within which the event occurs. The second component is the time at which the event occurs within the specific clock cycle of the reference clock.

Chen does not teach or suggest a timestamp or the act of timestamping events with a resolution of less than one clock cycle. Chen teaches a timestamp for a block of data, and the timestamp is derived from an internal clock 58. One with normal skill in the art would recognize that a typical system internal clock depends upon counting an integral number of clock cycles, and thus would have a resolution that is not less than a clock cycle. Thus, Claims 1 and 10 are patentable over Chen.

Claims 1-5 and 10-14 are currently rejected under 35 U.S.C. 102(b) as being anticipated by Adelman et al. (US 4894823). In response, Claims 1-5 and 10-14 have been amended to more clearly distinguish the present claimed invention from Chen. Specifically, Claims 1 and 10 have been amended to include timestamping an event with a resolution of less than one clock cycle.

Adelman is directed to timestamping packets in a network, and as such relies on a local time signal. One with normal skill

in the art would recognize a local time signal as being derived from an integral number of clock signals, and Adelmann is silent with respect to the generation of a time stamp with a resolution of less than one clock cycle.

Claims 26-32 are currently rejected under 35 U.S.C. 102(b) as being anticipated by Fransson (US 5940467). In response, Claim 26-32 has been amended to clearly distinguish the present claimed invention from Fransson. Specifically, Claim 26 has been amended to recite a circuit for timestamping events with a resolution of less than one clock cycle. Fransson is silent with respect to timestamps or timestamping.

Claims 20-25 and 40-41 are currently rejected under 35 U.S.C. 102(e) as being anticipated by Boerker (US 2003/0035502 A1). In response, Claims 20-25 have been amended to more clearly distinguish the present claimed invention from Boerker, and Claims 40-41 have been canceled. Specifically, Claims 20-25 have been amended to include timestamping an event with a resolution of less than one clock cycle.

Boerker is directed to the manipulation of a data stream and as such does not teach or suggest the timestamping of events with a resolution of less than one clock cycle.

Claims 6-9, and 19 are currently rejected under 35 U.S.C. 103(a) as being unpatentable over Adelman (US 4894823) in view of Boerker (US 2003/0035502 A1). In response, Claims 6-9 and 19 have been amended to patentably distinguish the present claimed invention from the combination of Adelman and Boerker. Specifically, Claims 6-9, and 19 have been amended to include timestamping an event with a resolution of less than one clock cycle.

Adelman and Boerker are directed to the handling of data as packets or streams, and are not concerned with the timing of events with a resolution of less than a clock cycle. One with normal skill in the art would recognize that the clocks relied upon by Adelman and Boerker would not have a resolution of less than one clock cycle, as claimed in Claims 6-9 and 19.

Claims 15-18 are currently rejected under 35 U.S.C. 103(a) as being unpatentable over Adelman (US 4894823) in view of Fransson

(US 5940467). In response, parent Claim 10 of Claims 15-18 has been amended to patentably distinguish the present claimed invention from the combination of Adelmann and Fransson. Specifically, Claim 10 has been amended to include timestamping an event with a resolution of less than one clock cycle. As described above, Adelmann and Fransson fail to teach or suggest timestamping events with a resolution of less than one clock cycle.

Claims 33-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fransson (US 5940467) in view of Boerker (US 2003/0035502 A1). In response, Claims 33-39 have been canceled.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boerker (US 2003/0035502 A1) in view of Fransson (US 5940467). In response, Claim 42 has been canceled.

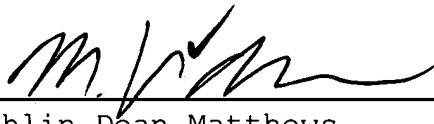
In summary, Applicant asserts that Claims 1-32 are now in condition for allowance and earnestly solicit such action by the Examiner.

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Respectfully submitted,

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